CLAIMS

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1. A two-bit non-volatile memory transistor comprising:

a semiconductor region having a first conductivity type;

a first source/drain region located in the semiconductor region, the first source/drain region having a second conductivity type, opposite the first conductivity type;

a second source/drain region located in the semiconductor region, the second source/drain region having the second conductivity type, wherein a channel region of the first conductivity type is located between the first and second source/drain regions;

a gate dielectric layer located over the channel region and portions of the first and second source/drain regions;

a first floating gate electrode located on the gate dielectric layer over the channel region and the first source/drain region, wherein the first floating gate electrode stores charge representative of a first data bit;

a second floating gate electrode located on the gate dielectric layer over the channel region and the second source/drain region, wherein the first and second floating gate electrodes are separated by a gap over the channel region, and wherein the second floating gate electrode stores charge representative of a second data bit;

a dielectric layer located over the first floating gate electrode and the second floating gate electrode; and

a control gate located over the dielectric layer.

2. The 2-bit non-volatile memory transistor of Claim 1, wherein the first and second floating gate electrodes comprise polysilicon.

3. The 2-bit non-volatile memory transistor of Claim 1, further comprising:

a first diffusion bit line continuous with the first source/drain region; and

a second diffusion bit line continuous with the second source/drain region.

4. The 2-bit non-volatile memory transistor of Claim 3, further comprising:

a first oxide region located over the first diffusion bit line; and

a second oxide region located over the second diffusion bit line.

5. The 2-bit non-volatile memory transistor of Claim 4, wherein a portion of the first floating gate electrode is located over the first oxide region, and a portion of the second floating gate electrode is located over the second oxide region.

6. The 2-bit non-volatile memory transistor of Claim 5, further comprising:

a first oxide layer located on an edge of the first floating gate electrode located over the first oxide region; and

a second oxide layer located on an edge of the second floating gate electrode located over the second oxide region.

7. The 2-bit non-volatile memory transistor of Claim 1, wherein a first portion of the control gate extends into the gap between the first and second floating gate electrodes.

8. The 2-bit non-volatile memory transistor of Claim 7, wherein the first portion of the control gate is separated from the channel region by the dielectric layer and the gate dielectric layer.

9. The 2-bit non-volatile memory transistor of Claim 1, wherein the control gate comprises polysilicon and metal silicide.

10. The 2-bit non-volatile memory transistor of Claim 1, wherein the gate dielectric layer comprises silicon oxide, and the dielectric layer comprises a first silicon oxide layer, a silicon nitride or silicon oxynitride layer located over the first silicon oxide layer, and a second silicon oxide layer located over the silicon nitride or silicon oxynitride layer.

11. A method of operating a 2-bit non-volatile memory transistor having a control gate, a first floating gate and a second floating gate, the method comprising:

programming the first floating gate by hot electron injection using a first set of programming voltages, wherein the second floating gate is in an erased state when the first floating gate is programmed; and

programming the second floating gate by hot electron injection using a second set of programming voltages, wherein the first floating gate is in a programmed state when the second floating gate is programmed, and wherein the first set of programming voltages includes a first voltage applied to the control gate, and the second set of programming voltages includes a second voltage applied to the control gate, the second voltage being higher than the first voltage.

12. The method of Claim 11, wherein the first voltage is about 1-2 Volts, and the second voltage is about 3-4 Volts.

13. The method of Claim 11, further comprising:

erasing the first floating gate by applying a first erase voltage to the control gate and a second erase voltage to a first source/drain region of the transistor, thereby removing electrons from the first floating gate; and

erasing the second floating gate by applying the first erase voltage to the control gate and the second erase voltage to a second source/drain region of the transistor, thereby removing electrons from the second floating gate.

14. The method of Claim 11, further comprising:

reading the state of the first floating gate by applying a first set of read voltages to the transistor; and

reading the state of the second floating gate by applying a second set of read voltages to the transistor, wherein the first set of read voltages includes a first read voltage applied to a first source/drain region of the transistor and a second read voltage applied to a second source/drain region of the transistor, and wherein the second set of read voltages includes the first read voltage applied to the second source/drain region and the second read voltage applied to the first source/drain region.

15. The method of Claim 11, further comprising erasing the first and second floating gates by exposure to ultra-violet light.

16. A method of fabricating a 2-bit non-volatile memory transistor, comprising:

forming a gate dielectric layer over a semiconductor substrate having a first conductivity type;

forming floating gate layer over the gate dielectric layer;

removing a first portion of the floating gate layer, thereby creating an opening through the floating gate layer;

forming a dielectric layer over the floating gate layer, wherein a portion of the dielectric layer

extends into the opening and onto the gate dielectric layer;

removing a second portion of the floating gate layer, thereby creating first floating gate and a second floating gate, wherein a first opening is located adjacent to the first floating gate, and a second opening is located adjacent to the second floating gate;

implanting impurities having a second conductivity type, opposite the first conductivity type, into the substrate, through the first and second openings;

thermally growing oxide on the substrate and sidewalls of the first and second gate electrodes through the first and second openings; and

depositing a control gate over the dielectric layer and the oxide.

17. The method of Claim 16, wherein the dielectric layer comprises a silicon oxide layer and a silicon nitride or silicon oxynitride layer located over the silicon oxide layer.

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